



Towards energy-saving chips for digital, analog, RF

The FAMES Pilot Line of the Chips JU is funded by Horizon Europe and Digital Europe Programmes and the National Public Authorities of the partners involved.




Ministry of Science and Higher Education
Republic of Poland



GOBIERNO
DE ESPAÑA

MINISTERIO
PARA LA TRANSFORMACIÓN DIGITAL
Y DE LA FUNCIÓN PÚBLICA

 Bundesministerium
Klimaschutz, Umwelt,
Energie, Mobilität,
Innovation und Technologie



PERTE
Chip



LAND  KÄRNTEN



ZUKUNFTSFONDS
STEIERMARK

European Chips Act 5 Pilot Lines

Nano IC: European pilot line for beyond 2nm leading edge system-on-chip leadership

APECS: Advanced Packaging for Electronic Components and Systems and Heterogeneous Integration

FAMES: FD-SOI pilot line for Applications with non-volatile embedded Memories, RF & 3D integration for European Sovereignty

PIXEurope: Advanced Photonic Integrated Circuits Pilot Line for Europe

WBG: Wide Band Gap materials pilot line - GaN & SiC



Consiglio Nazionale delle Ricerche

FAMES Pilot Line: Aim & Status

- The FAMES Pilot Line will provide opportunities for disruptive chips architecture with performance improvement and significant energy savings
- All Pilot Line agreements completed in December 2024, project is running at full speed (procurements, R&D programs, communication & dissemination)
- First Open Access call (request for Access) in March 2025

Consortium



FAMES Pilot Line Consortium

- Hosting sites
- Skills contributors

Budget : €830 M

- CAPEX: €382 M
- OPEX: €448 M

Funding:

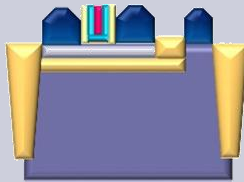
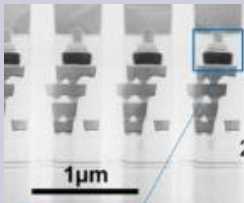


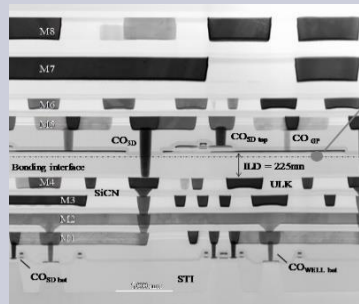
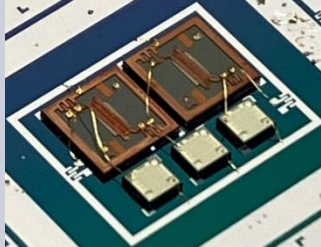

















- 50% Chips JU
- 50% Member States



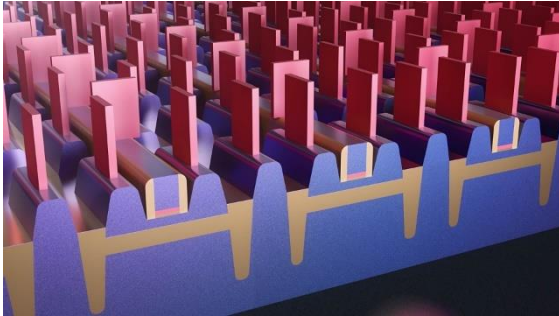
fames-pilot-line.eu



FAMES Technological Portfolio

FD-SOI	Embedded non-volatile memories	Radiofrequency components	3D integration	Small inductors for DC-DC converters
<p>10 nm and 7 nm nodes</p>  <p>0,7V 57CPP 48/40MPP</p>	<p>OxRAM, FeRAM, MRAM and FeFET</p>  	<p>Switches, filters, and capacitors</p> 	<p>Heterogeneous and sequential</p> 	<p>Power management integrated circuits (PMIC)</p> 
   	      	  	 	

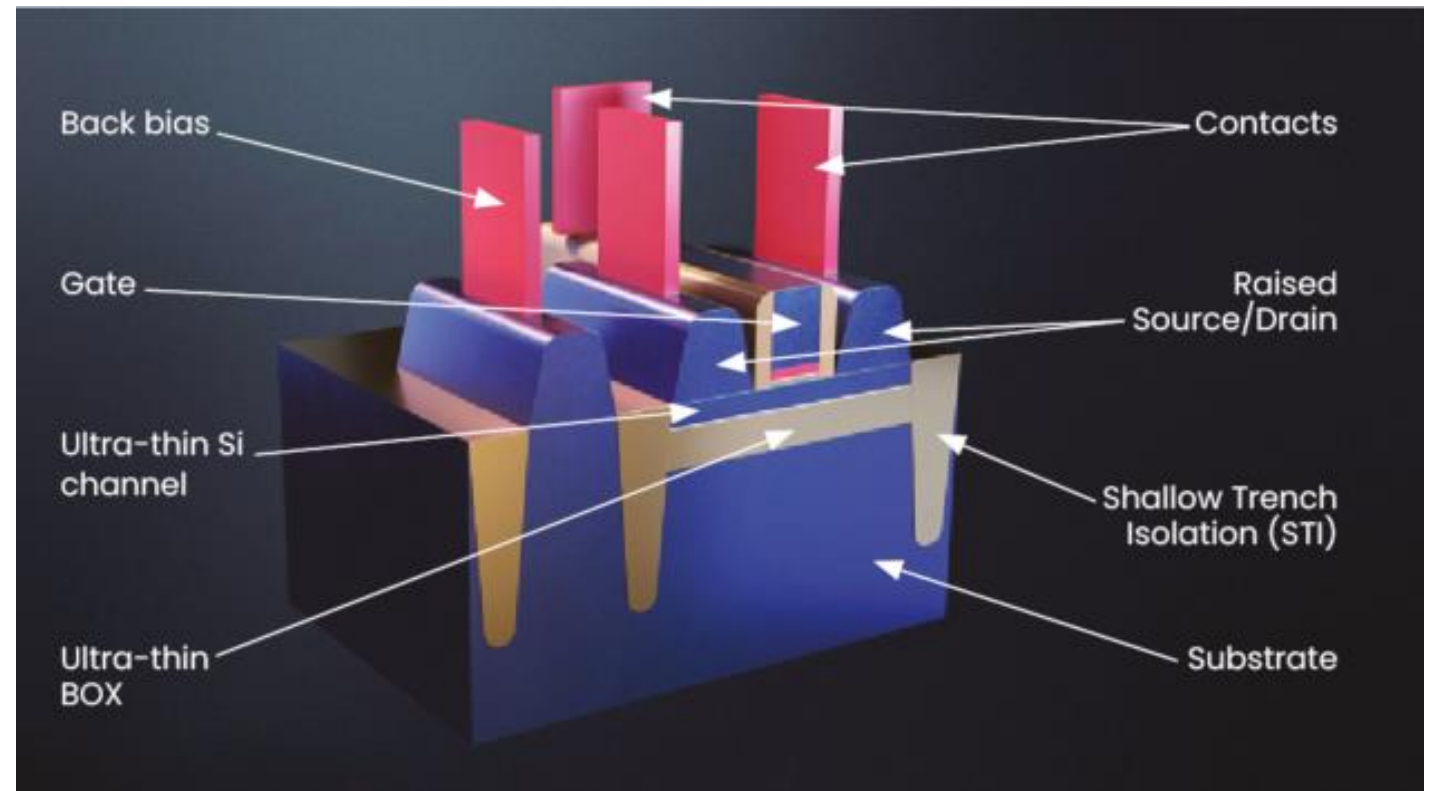
FD-SOI 10nm and 7nm nodes



- Transistor density
- High-performance/low-power trade-off
- Radiation resistance
- Reduced current leakage
- Manufacturing costs

- Over **150 patents** filed by CEA-Leti

An innovative generation of chips with the best balance in Power, Performance, Area, Cost and Environment (PPAC-E) for highly energy efficient applications



FD-SOI is selected by worldwide key players



Communications

- FD-SOI is ideal for 5G mmWave
- 5G sub-6 GHz
- Mobile infrastructure
- WiFi 6



November 2021
Google Pixel 6 5G mmW
with Samsung FD-SOI



August 2022
Next gen 5G mmw RFIC
by Qualcomm will use 22FDX
technology



July 2022
MediaTek 5G mmWave platform
uses 22 FDX



April 2023
Nordic redefines its leadership
in Bluetooth Low Energy with the
announcement of the nRF54 Serie



Automotive

- Autonomous cars
- Infotainment



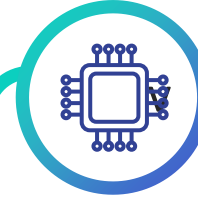
March 2021
Bosch mmW radar ECSEL
projet OCEAN 12



March 2021
NXP for ultra-low power
in automotive



ST unveils its new MCU Stellar
MCU for Auto



Smart Devices

- Edge computing
- 3D sensing & healthcare
- Smart home & smart cities
- Data centers



January 2022
NXP for ultra-low power
in automotive



GNSS
Development of 0.7 V RF circuits
with efficient energy use



GPS
The watch launched by the
company Huami features a GPS
circuit built on FD-SOI

Innovative, Differentiated Developments for Key Markets

Computing

- Microcontrollers
- MPU
- Trusted IC
- AI/ML chips

Sovereignty fields

- Quantum chips
- CryoCMOS chips
- Trusted IC
- New space components

More Than Moore

- Automotive
- 5G/6G chips
- RF connectivity
- Smart sensors
- Smart imagers
- Smart displays
- IoT devices
- Cybersecurity
- Wearables

Opening the Pilot Line to European stakeholders

44 support letters



FAMES Eco Innovation Offer

What expertise do industrial partners receive?

Materials:

- Solutions to reduce, replace, and recycle materials and to implement circular economy principles.
- Critical raw materials (CRM) analysis.

Technologies and systems:

- Eco-innovation to leverage the advantages of ecodesign and to mitigate the factors contributing to the climate crisis
- Analysis of value chains and rebound effects to reduce overall environmental impacts.

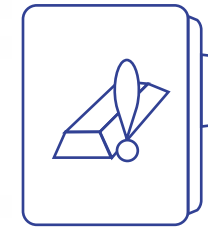


FAMES Eco Innovation Offer

Eco-innovation for more sustainable electronics
 Reducing the impacts of electronics through R&D



E-waste



Critical Raw Materials



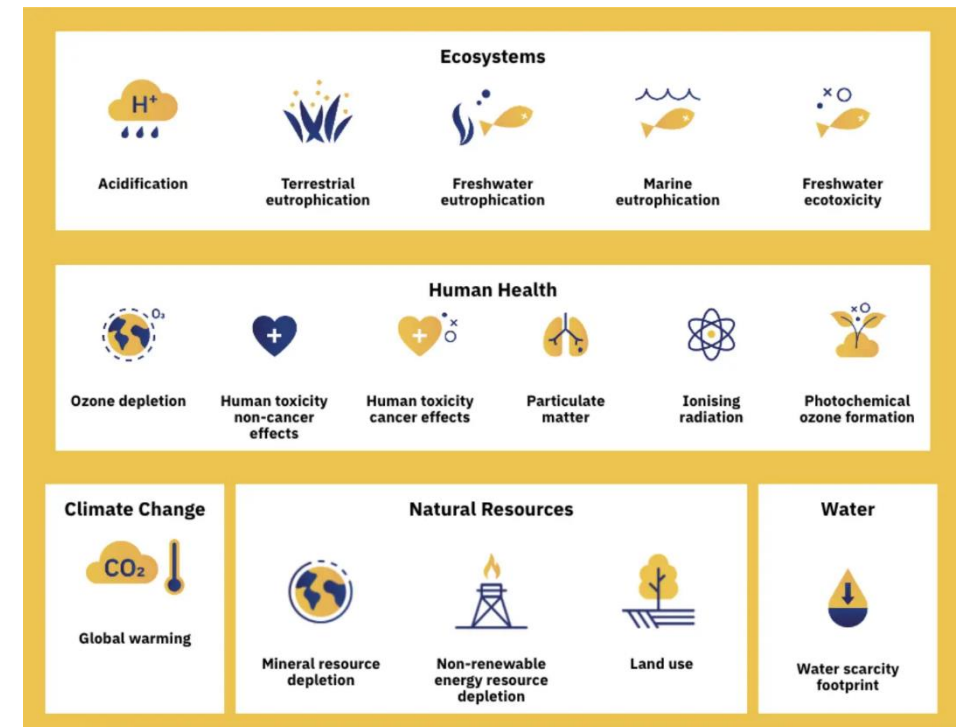
Planetary boundaries



Environmental regulations

- The development and implementation of **lifecycle analysis (LCA)**
- The validation of eco-innovative solutions in a production-like environment
- The development of technologies and end-to-end systems to meet specific environmental criteria for identified use cases.

16 environmental footprint criteria





Accessing the FAMES Pilot Line



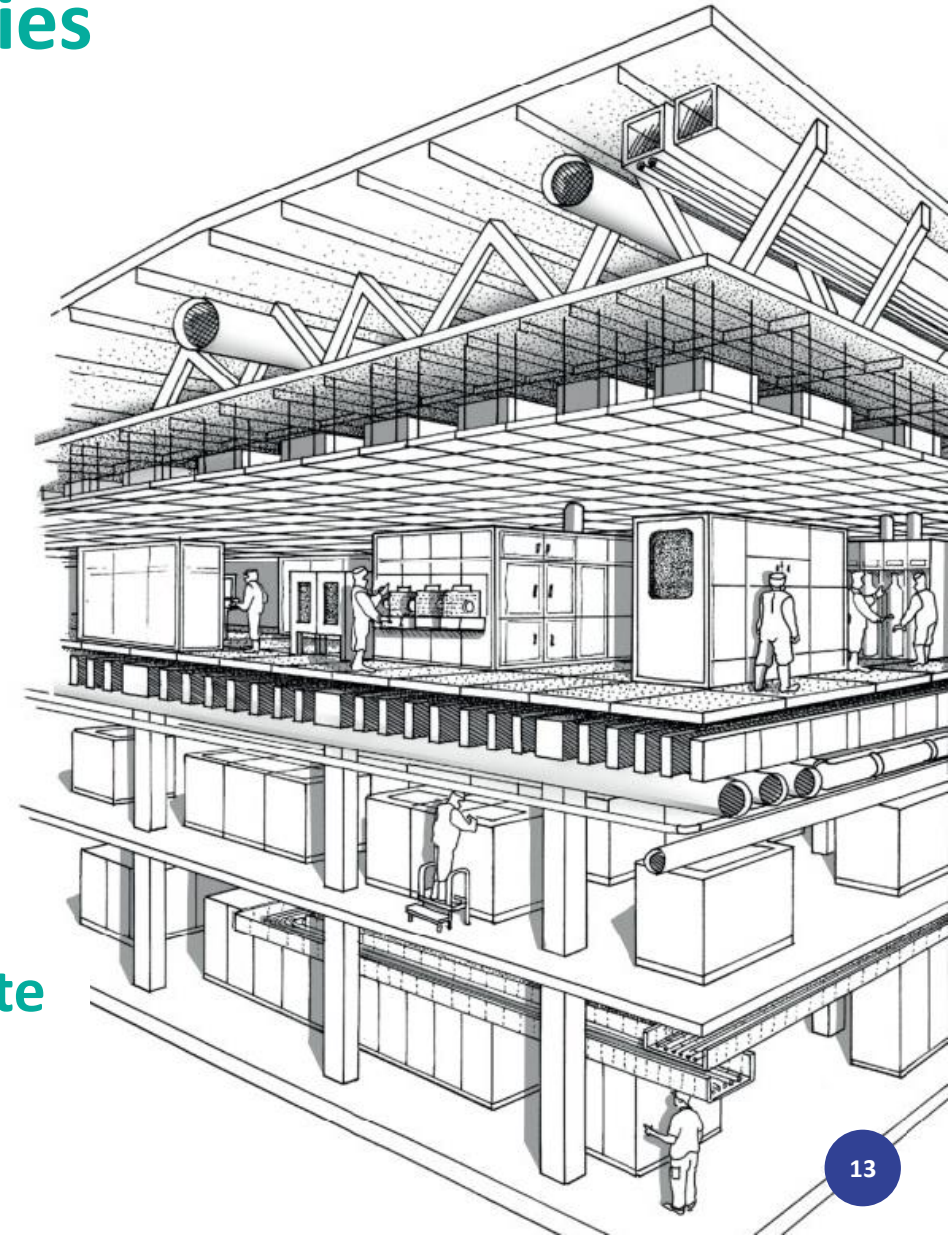
FAMES European open-access pilot line for advanced semiconductor technologies

To gain access to:

- Two types of PDKs (multi-project wafer or IC design assessment)
- The FAMES technologies (FD-SOI 10 nm and 7 nm, embedded non-volatile memories, RF components, 3D integration options) for performance evaluation
- Specific process steps, modules, integration flows, and demonstrator results
- Education and training on the FAMES technologies

as they become available

➔ Request an access to the Pilot Line and receive a quote



The FAMES Pilot Line is open to all types of Users



LARGE COMPANIES



SMEs



START-UPS



RESEARCH COMMUNITY



Design Houses

Fabless

Foundries

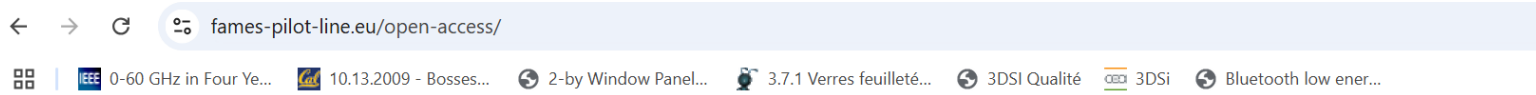
Integrated Device Manufacturers

Material and Tool Suppliers

Universities

Research Centers


Open Access calls: request for Access to the Pilot Line



OPEN ACCESS

FAMES Pilot Line

The FAMES pilot line offers European semiconductor stakeholders from industry, research, and academia access to a wide range of semiconductor technologies, including testing, PDKs, demonstrators and manufacturing capabilities.



Title: FAMES Pilot Line User Guidelines and Procedures
Author: S. Bonnetier et al
Version: 07

FAMES PILOT LINE USER GUIDELINES AND PROCEDURES

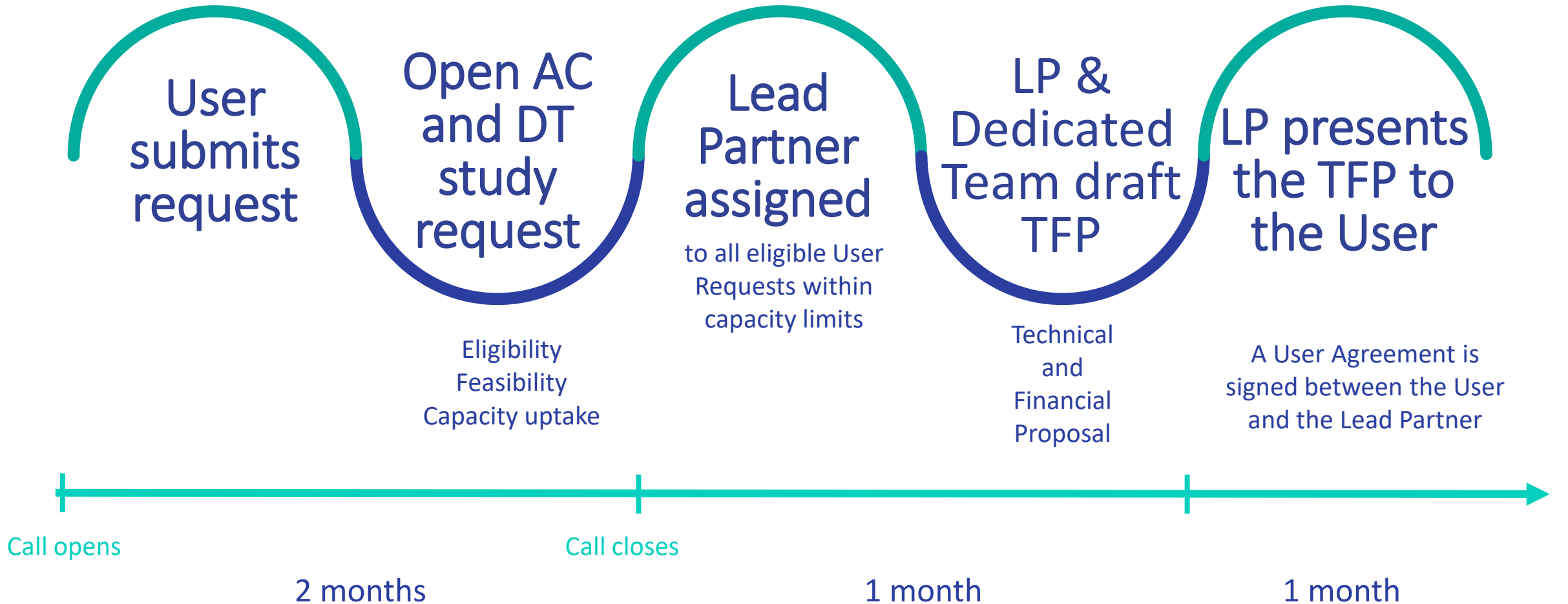
Project Number	101182279	Project Acronym	FAMES
Project Title	FD-SOI Pilot Line for Applications with embedded non-volatile Memories, RF, 3D integration and PMIC, to ensure European Sovereignty		



Open calls

The first call should open by the spring of 2025. You will find the submission details on this page as soon as the call is open.

Open Calls: User Request timeline



Approximate timeline

Access form – User Request for access to the Pilot Line

- Name and email of the person submitting the request
- Position in the organisation
- Organisation name and address (country from a pull-down menu)
- Organisation's website address
- Organisation type (pull down menu – large group, SME, Start-up, Academic)
- Organisation's activity sector (pull down menu)
- Technologies requested (pull down menu)
 - Portfolio technologies you are requesting (pull-down menu)
 - Other technologies you are requesting
- Comments/Explanations
- How did you hear about FAMES Pilot Line? (pull-down menu)
- “I agree with the Personal Data Protection policy of this Open Call”

Forthcoming Key Dates

Mid-March, 2025

**FAMES Pilot Line
Open Call
(Request for Access)**
Online opening



fames-pilot-line.eu

March 18, 2025

**FAMES Dedicated
Workshop**
Launch of the 1st open call
Brussels, Belgium



fames-pilot-line.eu

June 19, 2025

**FAMES
School**
Initial training
Grenoble, France



leti-innovation-days.com

The CEA logo consists of the lowercase letters 'cea' in white, positioned inside a red square. A thin white horizontal line is located directly beneath the 'a'.

cea

leti



Leti Innovation Days

June 17-19, 2025 | Grenoble, France

leti-innovation-days.com

Contact: bruno.paing@cea.fr



PARTNER WITH US
to fast track
your innovation project